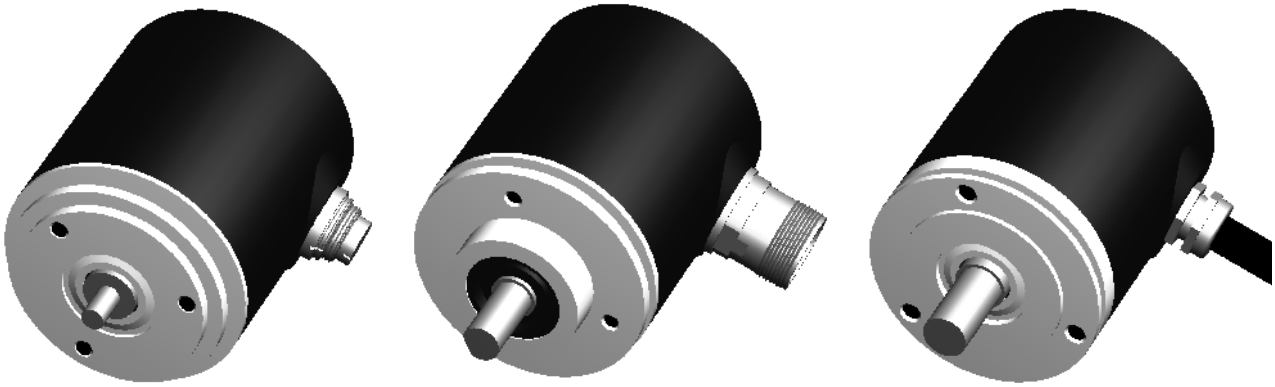
DESCRIPTION OF THE SYSTEM



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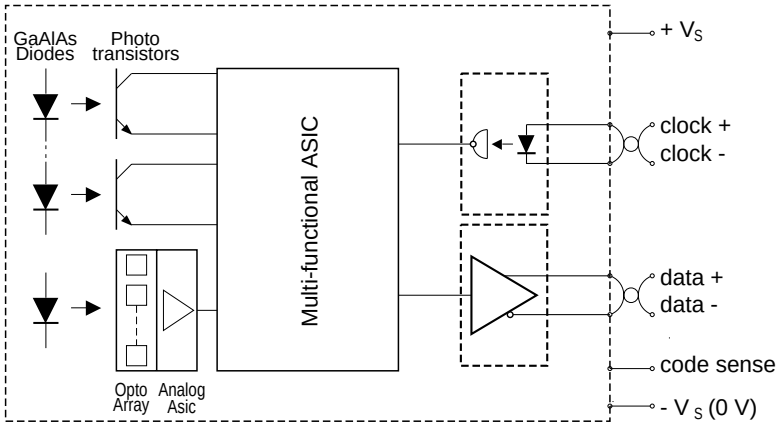
1. Advantage of the *SSI* over parallel interfaces

- **Significantly less expenditure for cabling: In the case of 24 bit encoders, only 4 lines are needed for the transmission of data instead of 24.**
- **Expenditure for cabling and interface components does not depend on the length of the data word.**
- **Screening out of noise is achieved through the clock and data signals being transmitted synchronously and symmetrically via twisted pair lines.**
- **Multiple transmission of each data word provides an automatic plausibility check.**
- **Absolute Encoder and reception electronics are separated with opto-couplers rendering earthing loops unnecessary.**

2. Mode of functioning and block diagram of the *SSI*

The parallel information in the encoder is converted by an internal parallel-serial converter (shift register) into serial form and is transmitted to a reception electronics unit synchronously with a clock.

Block diagram of a multiturn absolut encoder



The synchronized transmission of each data word is initiated and controlled by the reception electronics with the aid of a clock signal. The length of the **clock sequence (sequence of clock signals)** determines the length of the data word so that data words of any desired length can be transmitted with this *SSI* system. A clock sequence of n + 1 cycles is needed to transmit a data word with n bits. The speed of transmission is determined by the clock frequency.

3. Savings in lines with *SSI*

In the case of a multiturn encoder with parallel output and, for example, 4096 positions/revolution and 4096 revolutions (24 bit), 24 wires are needed to transmit the data. The *SSI*, on the other hand, requires only one twisted pair line for the data (data+, data-) and one twisted pair line for the clock (clock+, clock-). The line requirements for operating voltage and additional functions (e.g. code sense) are the same in both cases. As a minimum a cable with 6 wires (clock, data and supply voltage) is required.

4. Transmission protocol

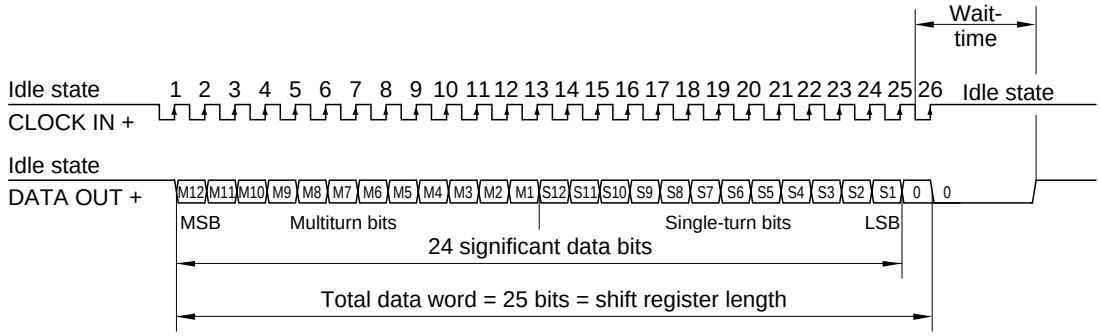
The logic levels as mentioned in the text relate to the clock + or, as the case may be, data + signal. In the idle or initial state of the *SSI* , both clock and data lines (clock +, data +) are Log 1. The reception electronics initiates the transmission of data by changing the clock signal from Log 1 to Log 0. This change causes a retriggerable monoflop in the encoder to be set. In turn the output from the latter switches over a shift register from parallel to serial whereby the data, which is present in parallel form in Gray code is stored.

The next time the clock changes from Log 1 to Log 0, the most significant bit of the angular position information is transferred to the data output of the encoder. Each further positive edge then causes the next highest bit in each case to be transferred until the least significant bit is at the output. At the same time the monoflop is retriggered with each negative edge of the clock.

The monoflop time (e.g. 20 µs) determines the interval between two transmissions and the minimum clock frequency.

SSI interface profile - 25 bit

Example: Absolute Encoder with 4096 positions / 360°, 4096 revolutions and Gray tree as output code



The data line is set to Log 0 with the last positive edge of the clock sequence. This terminates the transmission of the complete data word. If the clock signal remains set at Log 1 (end of the clock sequence), the monoflop is no longer retriggered so that the data signal switches to Log 1 on the expiration of the monoflop time.

This state indicates the readiness to transmit a new data word (simple transmission of one data word).

If the clock sequence is not terminated after the transmitting of the least significant data bit, the standard situation is that a Log 0 is issued on the data line with the next positive edge. This intermediate clock signal separates one data word from an identical data word that it follows. The positive edge following the intermediate clock signal edge generates the most significant bit of the data word (repeat transmission of the same data word). This process can be repeated as often as desired (multiple transmission of one data word). Alternatively the *SSI* can be arranged in such a way that the data signal remains at Log 0 after the data word has been transmitted once even if further clock signals follow.

5. Transmission example for an encoder with 18 bits

Encoder with 1024 positions/revolution (10 bits in the single-turn part) and 256 revolutions (8 bits in the multiturn part).

In the standard version, the transmission protocol is set up for a data word with 25 bits. Of these 12 bits are for the revolutions and 13 for the resolution (positions/revolution).

Since transmission always starts with multiturn bit M12 whereby however in our example the multiturn part is only designed for 8 bits, 4 blanks are first transmitted with Log 0 and then the loaded 8 bits of the multiturn part are transmitted. Then follow the single-turn bits starting with S10 and going to S1. Finally Log 0 is also transmitted for the last three bits which are not loaded.

Data word with n = 25

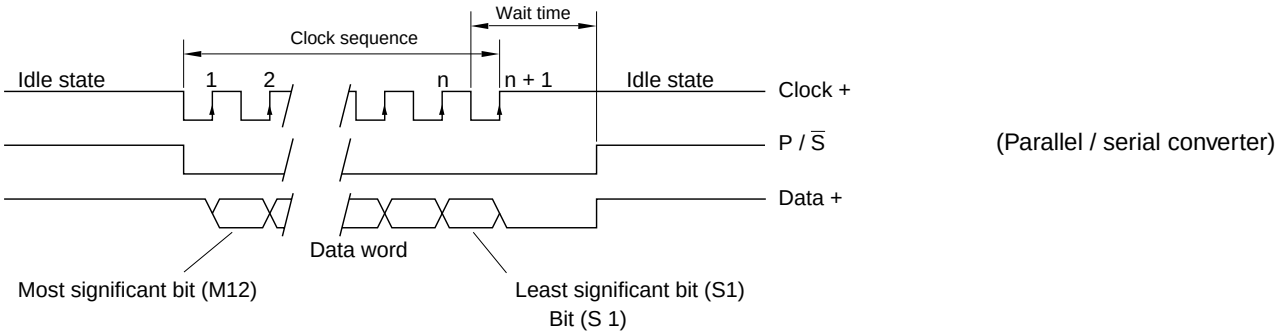
Bit No. in data word

MSB LSB

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25		
4096	12	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	8192	13
2048	11	0	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	0	4096	12
1024	10	0	0	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	0	0	2048	11
512	9	0	0	0	M9	M8	M7	M6	M5	M4	M3	M2	M1	**S10**	**S9**	**S8**	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**0**	**0**	**0**	**1024**	**10**
256	**8**	**0**	**0**	**0**	**0**	**M8**	**M7**	**M6**	**M5**	**M4**	**M3**	**M2**	**M1**	S9	S8	S7	S6	S5	S4	S3	S2	S1	0	0	0	0	512	9
128	7	0	0	0	0	0	M7	M6	M5	M4	M3	M2	M1	S8	S7	S6	S5	S4	S3	S2	S1	0	0	0	0	0	256	8
64	6	0	0	0	0	0	0	M6	M5	M4	M3	M2	M1	S7	S6	S5	S4	S3	S2	S1	0	0	0	0	0	0	128	7
32	5	0	0	0	0	0	0	0	M5	M4	M3	M2	M1	S6	S5	S4	S3	S2	S1	0	0	0	0	0	0	0	64	6
16	4	0	0	0	0	0	0	0	0	M4	M3	M2	M1	S5	S4	S3	S2	S1	0	0	0	0	0	0	0	0	32	5
8	3	0	0	0	0	0	0	0	0	0	M3	M2	M1	S4	S3	S2	S1	0	0	0	0	0	0	0	0	0	16	4
4	2	0	0	0	0	0	0	0	0	0	0	M2	M1	S3	S2	S1	0	0	0	0	0	0	0	0	0	0	8	3
2	1	0	0	0	0	0	0	0	0	0	0	0	M1	S2	S1	0	0	0	0	0	0	0	0	0	0	0	4	2
Number of revs	Bits / rev.	Multiturn bits												Single-turn bits													Position / rev.	Bits / rev.

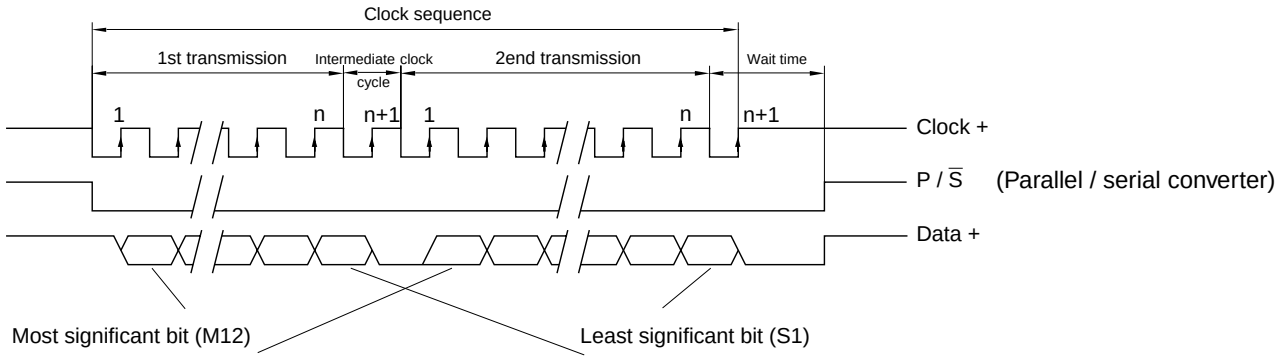
6. Single transmission

In the case of a single transmission, i.e. when the current position data is read out once, the clock sequence can be terminated after the transmission of the LSB since only zeroes will follow this.



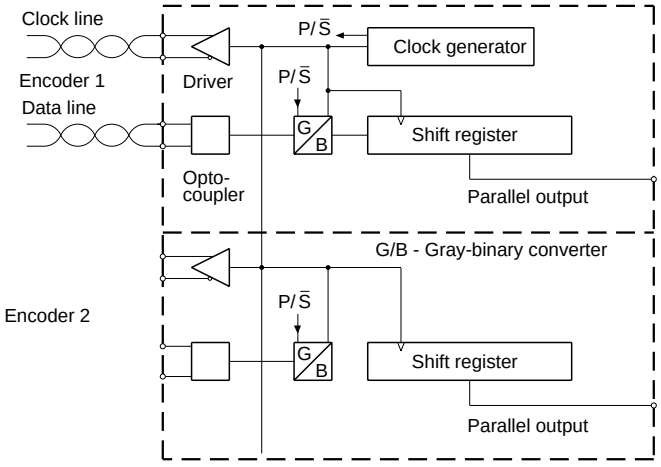
7. Multiple transmission

In the case of multiple transmission, i.e. when the current position data is read out a number of times, the clock sequence is designed in accordance with the schematic below.



8. *SSI* control electronics

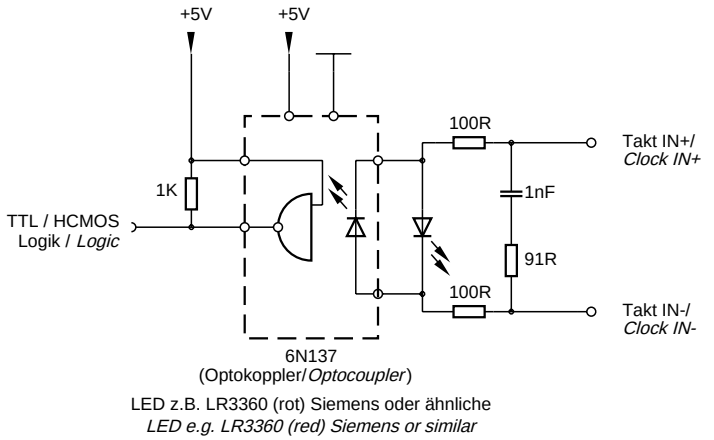
The control electronics generate the clock sequence with which the transmission of the data word from the encoder is regulated. In this unit the serial data can be converted back into parallel form and, if necessary, Gray code can be converted into natural binary code.



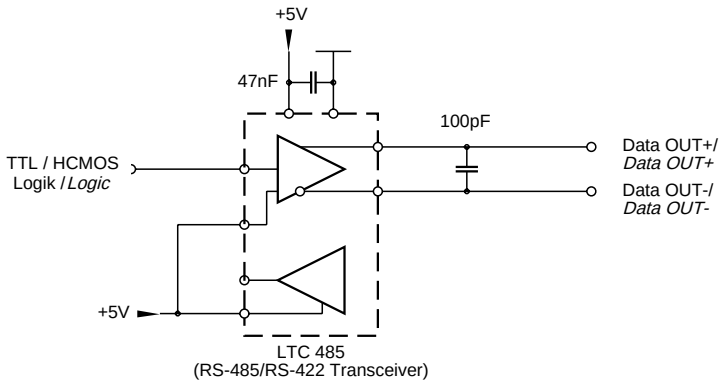
9. Input and output circuits

The input (opto-coupler) and output (line driver) circuits in the encoder and in the control electronics can be identical.

Input circuit



Output circuit



The output circuit is in the form of a differential line driver which fulfils complaying with RS 422 / RS 485. The differential, symmetrical design ensures a high degree of reliability in respect of noise. The use of opto-coupler inputs means that earth loops are not required and this in turn reduces the sensitivity to noise still further. This is especially important for situations where a number of encoders are connected to one control electronics unit.

10. Selection of the clock frequency and of the monoflop time

The monoflop, which is set by the first negative edge of the clock sequence, keeps the parallel/serial converter of the encoder in its active phase. For this reason it must remain set during the transmission phase and must be retriggered by each succeeding negative edge of the clock sequence. Accordingly the cycle time of the clock t_T must be shorter than the monoflop time t_M. The cycle time is the reciprocal of the clock frequency f_T.

$$t_T = \frac{1}{f_T} < t_M \text{ (min)}$$

In the standard version, the monoflop time t_M is set to 15 µs ≤ t_M ≤ 25 µs. The time t_M determines the minimum clock frequency f_T and the maximum wait time after the end of transmission t_W. t_W is calculated from the last negative flank of the clock and is identical with t_M. $t_W = t_M$

Example t_M = 10 µs to 30 µs

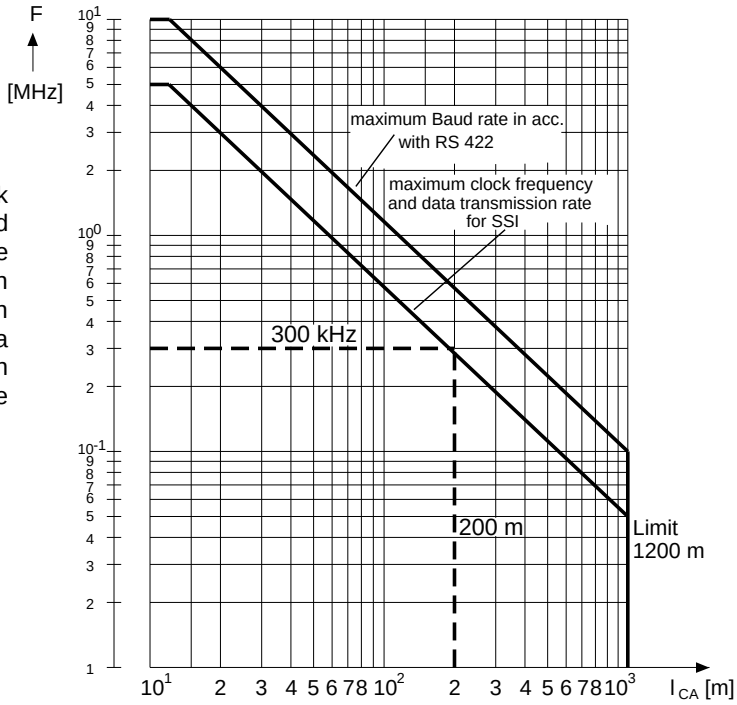
Accordingly: cycle time f_T ³ 1 / 10 µs = 100 kHz

Maximum wait time $t_W = t_M$ (max.) = 30 µs

11. Maximum data transmission rate

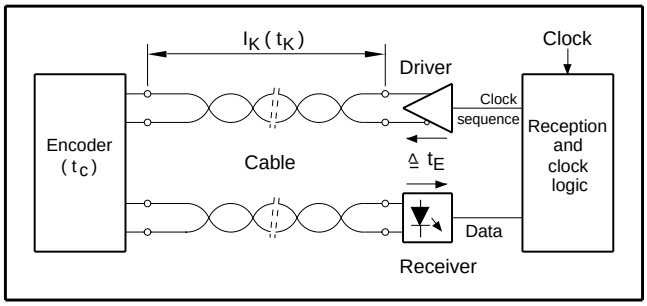
11.1 Preconditions

The maximum achievable data transmission rate (clock frequency) is set for the drivers and reception electronics used as well as for the transmission protocol in accordance with the RS 422 standard. It must be one half of the values stated in the standard for the Baud rate. Both limit curves are shown in the adjoining graph. It is shown below how the maximum data transmission rate can be achieved by means of measures on the reception electronics side by taking into account the different transit times.



11.2 Transmission link

The figure on the right shows in schematic form a *SSI* transmission link. It consists of encoder, transmission cable and clock sequence / reception electronics. Naturally each of these units has its own delay or transit time which delays the signals. This leads to the situation that the data reaches the reception side in time with the clock signals but delayed by the sum of the above-mentioned delay times.



11.3 Delay times of the individual units

In terms of delays, the complete *SSI* can be subdivided into three units:

- Encoder electronics
- Clock and data lines
- Reception and clock logic

The delay time of the first is constant and is specified for the encoder. The delay times for the last two depend on the particular application. The transit time in the cable varies with the length of the cable and the delay in the electronics depends on the logical units used.
Accordingly the following applies for the total delay (TD): $t_{TD} = t_C + 2 \times t_{CA} + t_E$

The cable delay has to be applied twice since not only the clock signal but also the data signal must pass along its full length.

The individual items in the above formula are:

t_{TD} : total delay time between clock and data signal.
t_C : delay brought about by the electronics in the encoder: for all TWK encoders it is specified as maximum 150 ns.

t_{CA} : cable delay; this delay depends on the length of the cable and also on the cable used. It is defined as the product of the cable length (l_{CA}) and the specific transit time for the cable. For the cable used by TWK, namely LIYCY-OB 4 x 2 x 0.25 mm², the specific transit time is approx. 6.5 ns/m.

t_E : delay time of the clock driver and of the data receiver (opto-coupler). For the TWK serial/parallel converter board SPC, it is specified to be maximum 150 ns.

Accordingly the above values can be inserted into the formula

$$t_{TD}\ (ns) = 300\ ns + 2 \times 6.5\ ns/m \times l_{CA}\ (m)$$

Example: For a cable of length 200 m the total delay is

$$t_{TD} = 300\ ns + 2 \times 6.5\ ns/m \times 200\ m = 2900\ ns = 2.9\ \mu s$$

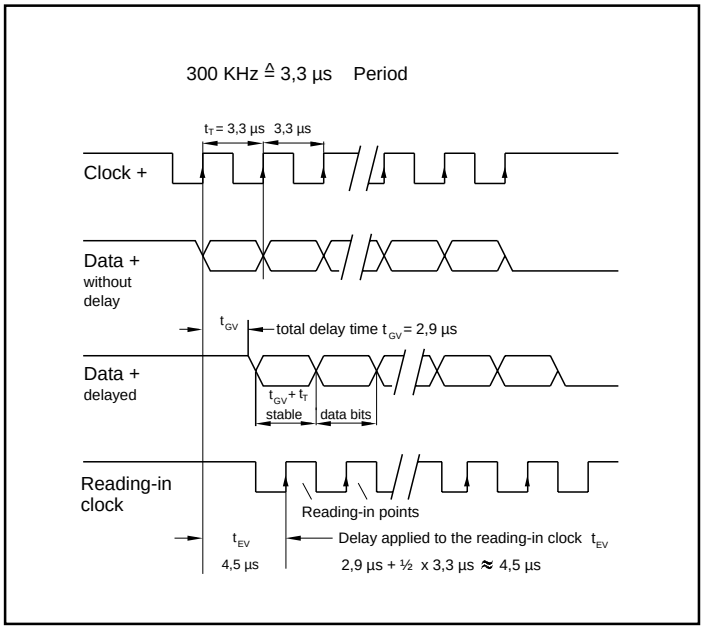
In the schematic below the significance of the total delay time t_{TD} for transmission is represented for the above example. The clock frequency selected is 300 kHz, namely the maximum permitted for a cable length of 200 m. This clock frequency is equivalent to a clock cycle time (t_T) of 3.3 µs.

11.4 Significance of the time by which the evaluation (reading-in) of the data as transmitted should be delayed

As has been shown above, the total delay time for the transmission of the data is of the same order of magnitude as the maximum possible length of the clock signal cycles.

If the data is to be processed correctly, it must be read in by the reception electronics at the right moment in time.

Since the period of time during which the individual data bits are present and stable on the reception side is identical with the clock cycle time, the reading in of the data must also take place during the same time period (see schematic below). In order to balance out tolerances in an optimum manner, the middle of this time period should be selected.



In order to maintain synchronism, the reading-in clock sequence should be the same as the data-transmission clock sequence but delayed relative to the latter by a suitable amount t_{EV} :

$$t_{TD} < t_{EV} < t_{TD} + t_T$$

In this range the data will be read in correctly with the positive edge. If reading in should take place in the middle of the time period, the following applies:

$$t_{EV} = t_{TD} + 1/2 \times t_T$$

This case is shown in the schematic above for the example given in 11.3.